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PATENT

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0002] of the specification as filed with the following:

[0002] As illustrated in the equivalent circuit diagram depicted in FIGURE 5A, integrated circuit comparators typically include: a bias system generating a defined current bias to each transistor; an input differential pair--either complementary metal oxide semiconductor (CMOS) or bipolar junction transistors--that, for a given overdrive voltage $V_{(ov)}=(V_{(inp)}-V_{(inn)})$ generate a differential current given by $I_{(ov)}=gm*V_{(ov)}$, where gm is the transconductance of the input differential pair at the steady-state operating point $V_{(ov)}=0$ volts (V); a gain stage node n_{gain} converting the current $I_{(ov)}$ to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current $I_{(ov)}$ available, the voltage excursion required between the high and low levels at the n_{gain} node, and the capacitive load at the n_{gain} node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

Please replace paragraph [0012] of the specification as filed with the following:

[0012] FIGURE 3 is a block diagram of a low power integrated circuit pulse generator and comparator according to one embodiment of the present invention; and

Please delete paragraph [0013] of the specification as filed.

Please replace paragraph [0014] of the specification as filed with the following:

[0014] FIGURE 5 4 is an equivalent circuit diagram of a typical integrated circuit comparator.

Please delete paragraph [0033] of the specification as filed.

Please cancel Figures 4A and 4B of the application as filed, and relabel Figure 5 as filed to Figure 4.